MappingTable Functional Description

This object is NOT an hardware component. It can be used by the system designer to describe the memory mapping and address decoding scheme of any hardware architecture build with the SoCLib hardware components.

All VCI initiatores and VCI targets share the same "flat" address space, but the address decoding scheme supports a multi-level structured interconnect.

One level interconnect

This is the simplest case:

- each VCI component is identified by a simple index.
- and all VCI targets must have different indexes. Most hardware interconnects (such as the make the assumption that the target indexes
- each VCI is identified by a simple index, and all initiators must have different indexes. The initiator index

must be equal to the VCI SRCID value.

- The VCI address is structured in two fields

Two level interconnect

The hardware architecture is supposed to be split into several subsystems (or clusters), with a global interconnect for inter-cluster communications, and one local interconnect in each cluster for intra-cluster communications.

- each VCI component is identified by a structured index containing two indexes:
    - ♦ a global index that is the subsystem (or cluster) index.
    - ♦ a local index, that identifies the VCI component in the cluster.
- All , and all targets must have different indexes. Most hardware interconnects (such as the make the assumption that the target indexes
- each VCI is identified by a simple index, and all initiators must have different indexes. The initiator index

must be equal to the VCI SRCID value.

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