

NiosII Processor Functional Description

This hardware component belongs to the NiosII embedded processor family designed for Altera® field programmable gate array (FPGA) devices. The NiosII processor is a configurable soft-core processor, as opposed to a fixed, off-the-shelf processor. ?Configurable? means that features can be added or removed on a system-by-system basis to meet performance goals. Altera® offers three NiosII cores:

- NiosII/f. The NiosII/f ?fast? core is designed for fast performance.
- NiosII/s. The NiosII/s ?standard? core is designed for small size while maintaining performance.
- NiosII/e. The NiosII/e ?economy? core is designed to achieve the smallest possible core size.

This hardware component is only an ISS, which should be wrapped with an IssWrapper.

The simulation model is actually an instruction set simulator, organized as a three-stage pipeline:

- First stage: instruction fetch, with access to the external instruction cache.
- Second stage: instruction is executed with a possible access to the external data cache.
- Third stage: read memory access is written back to registers

This component models the NiosII/f ?fast? core. Its main functional specifications are the following:

- Hardware multiplication and division are supported
- Floating-point instructions are supported by the way of custom instructions
- dynamic branch prediction is not supported
- optional tightly-coupled memory for instructions and data is not supported
- Load and store I/O instructions are not supported

Component definition

Available in source:trunk/soclib/desc/soclib/nios2_fast.sd

Usage

NiosII has no parameters.

```
Uses ( 'nios2_fast' )
```

NiosII Processor ISS Implementation

The implementation is in

- source:trunk/soclib/systemc/include/common/iss/nios2_fast.h
- source:trunk/soclib/systemc/src/common/iss/nios2_fast.cc
- source:trunk/soclib/systemc/src/common/iss/nios2_fast_itype_instructions.cc
- source:trunk/soclib/systemc/src/common/iss/nios2_fast_rtype_instructions.cc
- source:trunk/soclib/systemc/src/common/iss/nios2_fast_custom_instructions.cc

Template parameters

This component has no template parameters.

Constructor parameters

```
Nios2fIss(  
    sc_module_name name,    // Instance Name  
    int ident);             // processor id
```

Visible registers

The following internal registers define the processor internal state, and can be inspected:

- `r_pc` : Program counter
- `m_instruction` : Instruction register
- `r_gpr[i]` : General-purpose registers ($0 < i < 32$)
- `r_ctr[i]` : Control registers ($0 < i < 6$)
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Interrupts

NiosII defines 32 interrupt-request inputs. The lowest number has the highest priority.

Ports

None, it is to the wrapper to provide them.