

Ppc Processor Functional Description

This hardware component is a PPC405 processor core. This is only an ISS, which should be wrapped with an [IssWrapper](#).

The simulation model is actually an instruction set simulator, organised as a two-stage pipeline:

- First stage: instruction fetch & execute with a possible access to the external data cache.
- Second stage: read memory access is written back to registers

The main functional specifications are the following:

- The floating point instructions are not supported
- There is no TLB, and no hardware support for virtual memory

Component definition

Available in source:trunk/soclib/desc/soclib/ppc405.sd

Usage

Ppc405 has no parameters.

```
Uses ( 'ppc405' )
```

Ppc405 Processor ISS Implementation

The caba implementation is in

- source:trunk/soclib/systemc/include/common/iss/ppc405.h
- source:trunk/soclib/systemc/include/common/iss/ppc405_ops.inc
- source:trunk/soclib/systemc/src/common/iss/ppc405.cc
- source:trunk/soclib/systemc/src/common/iss/ppc405_instructions.cc
- source:trunk/soclib/systemc/src/common/iss/ppc405_jump_tables.cc
- source:trunk/soclib/systemc/src/common/iss/ppc405_instructions.cc

Template parameters

This component has no template parameters.

Constructor parameters

```
Ppc405Iss(  
    sc_module_name name,    // Instance Name  
    int ident);             // processor id
```

Ports

None, it is to the wrapper to provide them.