

!!!! UNDER CONSTRUCTION !!!!

## ST231 Processor Functional Description

The ST231 processor core is an hardware component implementing a 7-stage VLIW processor with register scoreboarding and 32-bit x 32-bit multiplies for integer and fractional data representations. Though a MMU was also added so the ST231 can be used as a host processor, this processor is mostly used in digital video consumer electronics.

This component is an ISS, which should be wrapped with an [IssWrapper](#) for integration into a complete platform.

This instruction set simulator acts as a slave to the [IssWrapper](#) and is organised identically to the other Isses available within the library.

## Component definition

Available in source: `trunk/soclib/soclib/lib/st231/metadata/st231.sd`

## Usage

ST231 has no parameters.

```
Uses ( 'microblaze' )
```

## Microblaze Processor ISS Implementation

The implementation is in

- `st231.hh`, `st231.cpp` : Defines the class `ST231Iss` which is the implementation of the ISS respecting the `IssWrapper` interface.
- `cpu/st231_isa.hh`, `cpu/st231_isa.cpp` : Implements the ST231 instruction set.
- `cpu/bundle.hh`, `cpu/bundle.cpp` : Implements the VLIW instruction bundle.
- `cpu/exception.hh`, `cpu/exception.cpp` : Implements the associated exceptions.
- `cpu/soclib_symtab.hh`, `cpu/soclib_symtab.cpp` : Implements the associated symbol table.
- `cpu/cpu_tlmt.hh`, `cpu/cpu_tlmt.cpp` : Implements the CPU including the 7-stage pipeline.

## Template parameters

This component has no template parameters.

## Constructor parameters

```
ST231Iss(  
    uint32_t ident          // processor id  
) ;
```

# Ports

The `IssWrapper` module is in charge of defining the communication ports.