SocLib Components General Index

TMS320C62 Processor Functional Description

This hardware component is a TMS320C62x core. The main features of the C62x CPU include:

- VLIW CPU with eight functional units, including two multipliers and six arithmetic units
- Instruction packing
- Conditional execution of all instructions

All instructions in the C62x DSP instruction set flow through the fetch, decode and execute stages of the pipeline. The fetch stage of the pipeline has four phases for all instructions and the decode stage has two phases for all instructions. The execute stage of the pipeline requires a varying number of phases, depending on the type of instruction. The pipeline can dispatch eight parallel instructions every cycle. Parallel instructions proceed simultaneously through each pipeline phase. Serial instructions proceed through the pipeline with a fixed relative phase difference between instructions.

This hardware component is only an ISS, which should be wrapped with a CABA or TLM-T Wrapper using the IssIss2 utility component.

It implements all instructions defined in the C62x architecture specification, with the following limitations:

- the C62x has internal (on-chip) memory, organized in separate data and program spaces, this feature is not supported

Component definition

Available in source:trunk/soclib/soclib/iss/tms320c6x/metadata/tms320c62.sd?

Usage

TMS320C62 has no parameters.

```
Uses( 'tms320c62')
```

TMS320C62 Processor ISS Implementation

The implementation is in

- source:trunk/soclib/soclib/iss/tms320c6x/include/iss/tms320c62.h?
- source:trunk/soclib/soclib/iss/tms320c6x/src/iss/tms320c62.cpp?
- source:trunk/soclib/soclib/iss/tms320c62/src/iss/tms320c62_decoding.cpp
- source:trunk/soclib/soclib/iss/tms320c6x/src/iss/tms320c62_instructions.cpp?

Template parameters

This component has no template parameters.

Constructor parameters

```
TMS320C62(
     sc_module_name name,   //  Instance Name
     int  ident);           // processor id
```

Interrupts

Ports

None, it is to the wrapper to provide them.

Compiling programs for TMS320C62 with SoClib

Free downloads of Texas Instruments Code Generation Tools for TMS320C6000 instruction set architectures produced by TI are available ?https://www-a.ti.com/downloads/sds_support/targetcontent/LinuxDspTools/download.html. These evaluation tools run on Linux x86 hosts.