Tc1700

1) Functional Description

This TC1700 is a flexible turbo decoder covering WiMAX, LTE and HSPA+ specifications provided by ?TurboConcept. Full documentation is available online at ?TurboConcept's Web Site.

TurboConcept's TC1700 Core is a turbo decoder that supports three PHY layer specifications:

- 3GPP-HSPA
- 3GPP-LTE
- WiMAX IEEE802.16e

The Core is optimized for ASIC and FPGA target and uses a unique architecture that reduces by more than 50 % the silicon area when compared to separate single-mode Cores, with no restrictions on the flexibility and features set.

Figure 1 presents the general core structure. The Tc1700 is connected to a MWMR wrapper in order to interface the core to the MWMR controller available at VciMwmrController.

2) CABA Implementation

a) Component definition & usage

- source:trunk/soclib/soclib/module/streaming_component/tc1700/caba/metadata/tc1700.sd
- source:trunk/soclib/binary/module/streaming_component/tc1700/caba/doc

b) CABA sources

- interface : source:trunk/soclib/soclib/module/streaming_component/tc1700/caba/source/include/tc1700.h
- implementation : source:trunk/soclib/soclib/module/streaming_component/tc1700/caba/source/src/tc1700.cpp
- internal component interface : source:trunk/soclib/binary/module/streaming_component/tc1700/caba/include/tc_tc1700.h
- internal component library : source:trunk/soclib/binary/module/streaming_component/tc1700/caba/lib

CABA Constructor parameters

- TC1700 decoder

```
Tc1700(
     sc_module_name name)                    // Instance name
```

CABA Ports

- sc_in<bool> **p_resetn** : hardware reset
- sc_in<bool> **p_clk** : clock

- soclib::caba::FifoOutput<uint32_t> **p_tc1700_to_MWMR** : interface from the tc1700 to the MWMR controller
- soclib::caba::FifoInput<uint32_t> **p_MWMR_to_tc1700** : interface from the MWMR controller to the tc1700

3) TLM-DT Implementation

a) Component definition & usage

- source:trunk/soclib/soclib/module/streaming_component/tc1700/tlmdt/metadata/tc1700.sd
- source:trunk/soclib/binary/module/streaming_component/tc1700/tlmdt/doc

TLM-DT sources

- interface : source:trunk/soclib/soclib/module/streaming_component/tc1700/tlmdt/source/include/tc1700.h
- implementation : source:trunk/soclib/soclib/module/streaming_component/tc1700/tlmdt/source/src/tc1700.cpp
- internal component interface : source:trunk/soclib/binary/module/streaming_component/tc1700/tlmdt/include/tc_tc1700.h
- internal component library : source:trunk/soclib/binary/module/streaming_component/tc1700/tlmdt/lib

TLM-DT Constructor parameters

```
Tc1700(
     sc_module_name name,    // Instance name
     uint32_t       id,
     uint32_t       MWMR2core_fifo_depth,
     uint32_t       core2MWMR_fifo_depth)
```

TLM-DT Ports

- std::vector<tlm_utils::simple_target_socket_tagged<Tc1700,32,tlm::tlm_base_protocol_types> *> **p_config**: configuration port
- std::vector<tlm_utils::simple_target_socket_tagged<Tc1700,32,tlm::tlm_base_protocol_types> *> **p_status**: status port
- std::vector<tlm_utils::simple_initiator_socket_tagged<Tc1700,32,tlm::tlm_base_protocol_types> *> **p_read_fifo**: port from the MWMR controller to the Tc1700
- std::vector<tlm_utils::simple_initiator_socket_tagged<Tc1700,32,tlm::tlm_base_protocol_types> *> **p_write_fifo**: port from the Tc1700 to the MWMR controller

4) Limitation

This model has the following limitations:

- fixed number of performed iterations.

The number of performed iterations is fixed to a reasonable value still offering close-to-ideal Bit Error Rate (BER) performances. Please contact ?TurboConcept for information about these limitations.

5) License

The MWMR wrapper is licensed under the SoCLib, GNU LGPLv2.1 license.

The MWMR wrapper instantiates an internal hardware decoder. This internal hardware decoder is licensed under BSD-like license.

This internal hardware decoder is distributed in a binary form.

6) RTL model

Please contact ?TurboConcept for information about purchasing a fully functional RTL model of the internal hardware decoder.