Tc4200

1) Functional Description

This VCI target corresponds to a IEEE802.16e LDPC decoder. It embeds an internal hardware Cycle Accurate Bit Accurate model of the ?TurboConcept's IEEE802.16e WiMAX LDPC decoder ?tc4200.

TurboConcept's TC4200-WiMAX Core is a high speed Low Density Parity Check code (LDPC) decoder optimized for WiMAX (IEEE 802.16e) specifications. A patented decoding architecture allows meeting high throughputs within small devices, and still offering close-to-ideal Bit Error Rate (BER) performances.

image(tc4200.png,align=right,nolink) Figure 1 - Tc4200?

Figure 1 presents the general core structure. The Tc4200 is made of a VCI wrapper and an internal hardware decoder model which communicates using proprietary FIFO-like protocols.

2) Component definition & usage

- source:trunk/soclib/soclib/module/streaming_component/tc4200/caba/metadata/tc4200.sd
- source:trunk/soclib/binary/module/streaming_component/tc4200/caba/doc

3) CABA Implementation

CABA sources

- interface : source:trunk/soclib/soclib/module/streaming_component/tc4200/caba/source/include/tc4200.h
- implementation : source:trunk/soclib/soclib/module/streaming_component/tc4200/caba/source/src/tc4200.cpp
- internal component interface : source:trunk/soclib/binary/module/streaming_component/tc4200/caba/include/tc_tc4200.h
- internal component library : source:trunk/soclib/binary/module/streaming_component/tc4200/caba/lib

CABA Constructor parameters

- IEEE802.16e LDPC decoder

```
Tc4200(
     sc_module_name name,                     // Instance name
     const soclib::common::IntTab &index,     //  Target index
     const soclib::common::MappingTable &mt)  // Mapping Table
```

CABA Addressable registers

- Read only registers
  - `TC4200_D_OUT` Data output register
  - `TC4200_MONITOR` Monitoring interface. See Figure 2 Image(monitor_reg.png,align=center, nolink) Figure 2 - Monitoring register.?
- Write only registers

- `TC4200_CONFIG` Configuration interface. See Figure 3 Image(config_reg.png, align=center,nolink) Figure 3 - Configuration register.?
- `TC4200_D_IN_FIRST` Register for the First data corresponding to a new frame. See Figure 4. Image(data_in_first.png, align=center,nolink) Figure 4 - First data of a new frame register.?
- `TC4200_D_IN` Register for any other input frame data. See Figure 5. Image(data_in.png, align=center,nolink) Figure 5 - Data register. Value for the i-th written data.?

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CABA Ports

- sc_in<bool> **p_resetn** : hardware reset
- sc_in<bool> **p_clk** : clock
- soclib::common::VciTarget<vci_param> **p_vci** : The VCI port

4) TLM-T Implementation

TLM-T sources

- interface : source:trunk/soclib/soclib/module/streaming_component/tc4200/tlmt/source/include/tc4200.h
- implementation : source:trunk/soclib/soclib/module/streaming_component/tc4200/tlmt/source/src/tc4200.cpp
- internal component interface : source:trunk/soclib/binary/module/streaming_component/tc4200/tlmt/include/tc_tc4200.h
- internal component library : source:trunk/soclib/binary/module/streaming_component/tc4200/tlmt/lib

5) Limitation

This model has the following two limitations:

- stopping criterion is disable;
- fixed number of performed iterations.

The number of performed iterations is fixed to a reasonable value still offering close-to-ideal Bit Error Rate (BER) performances. Please contact ?TurboConcept for information about these limitations.

6) License

The VCI wrapper is licensed under the SoCLib, GNU LGPLv2.1 license.

The VCI wrapper instantiates an internal hardware decoder. This internal hardware decoder is licensed under BSD-like license.

This internal hardware decoder is distributed in a binary form.

7) RTL model

Please contact ?TurboConcept for information about purchasing a fully functional RTL model of the internal hardware decoder.