

VCI_ANOC_Network

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1) vci_anoc_network overview

The vci_anoc_network is an interconnect module implementing the ANOC Network-on-Chip which is compatible with VCI interfaces.

1.1) ANOC Network on Chip

ANOC stands for Asynchronous Network-on-Chip (NoC) and has been developed by the CEA-Leti. ANOC is a wormhole packet switching NoC. Its architecture is composed by five ports routers interconnected by bidirectional links using send/accept asynchronous handshake protocol. Thus, the ANOC protocol offers naturally a GALS architecture. As the ANOC routers are asynchronous, the entire end-to-end path traveling the packets is completely asynchronous.

The ANOC topology is not reduced to regular 2D mesh. Irregular 2D mesh or 2D torus topology can also be implemented as ANOC uses a source routing algorithm. Moreover, source routing can be used to minimize the congestion on some links, and thus reduce the packet latency. A flit is the smallest flow control unit of the network. Each flit contains two control bits, Begin of Packet (BOP) and End of Packet (EOP). BOP is set on the head flit, and EOP is set on the tail flit. Furthermore, the first flit of the packet contains the routing information and the router uses this ?path-to-target? to decide the correct routing destination. The routing information is enclosed on 18-bits and two bits encodes each routing hop, which allows addressing a path of at most 9 router hops.

ANOC provides two virtual channels per NoC link. A low latency channel VC0 is provided for real-time applications and a higher latency and lower priority channel VC1 for best effort traffic.

1.2) vci_anoc_network specifications

The vci_anoc_network is a configurable interconnect implementing the ANOC network. In order to simplify the implementation of the ANOC Network, the vci_anoc_network module implements a regular 2D mesh topology of ANOC routers as shown in next figure. In this example, a 3x2 network is depicted. The big round represents the ANOC routers. Each ANOC router has attached a vci_anoc_wrapper (vaw) module which converts the ANOC protocol into the VCI protocol and vice versa.



The 2D mesh topology can have any width (W) and height (H)

The input and output ports of the vci_anoc_network module are:

- W*H VCI target ports
- W*H VCI initiator ports
- A clock signal
- A reset port

The configuration parameters allow to define the network width and height independently. All the ANOC routers and the VCI ports will be automatically allocated to satisfy the topology.

The ANOC router placed on the sides of the network do not have all their links connected with other ANOC routers. Thus, these links are connected to Stopper modules to detect error situations. If a Stopper module receives a packet, it will print a warning message.

The local port of the ANOC routers are connected to vci_anoc_wrapper modules which translate the VCI packets into ANOC transactions and vice versa.

The vci_anoc_network is intended to be used as a second order interconnect network in a hierarchic manner. It is strongly recommended to interconnect the initiator and target IPs of the same cluster through a local interconnect. Otherwise, the communication between initiator and target of the same cluster will be penalized by the local port of the network.



1.3) vci_anoc_wrapper

The vci_anoc_wrapper is a wrapper module that translate the VCI protocol into ANOC transactions. In the VCI side, it has two VCI ports, one initiator and one target port.

The vci_anoc_wrapper do not implement a bypass through the VCI initiator and the VCI target ports. Any request/response is directly send to the ANOC. Therefore, the vci_anoc_network should be used as a second order interconnect.

The VCI request/response commands are converted into ANOC packets of 38 bits per flit. This conversion is represented in the next table. The yellow areas are reserved areas. The first flit contains the ANOC routing path while the second flit contains the VCI address. The third flits encodes all the information of the request command. A VCI read request command requires only these three flits while a write request command requires additional data flits. The forth and following flits contains the data to write and its associated byte enable signals.



The VCI response packet is similar as the request packet. The first flit contains the ANOC routing path while the second contains the response information. The response packet to a VCI write request contains just two flits, while the response to a VCI read request contains the additional flits. The third and following flits are the read data of the read request command.



1.4) ANOC routing and traffic strategy

ANOC router can be used to implement non regular 2D mesh topologies. However, in this implementation, all the topologies are regular 2D.

- The ANOC router allow to use any of its 5 ports as the local IP port (where a vci_anoc_wrapper could be connected). In this implementation, only one port, the local router port, is used to connect the vci_anoc_wrappers.
- The ANOC router uses a source routing algorithm to route the packets over the network. In order to simplify the implementation while being deadlock free, the X-First routing algorithm is used. In each vci_anoc_wrapper, the VCI mapping table is used to determine the Destination cluster of a request/response command. The source routing path-to-target is computed with the X-First algorithm using two information: i) the Origin information provided by the [i,j] coordinates of vci_anoc_wrapper in the ANOC 2D topology and ii) the Destination information of the addressed cluster provided by the VCI mapping table.

- In a memory mapped system, request and response packets must be fully independent to provide a deadlock free NoC traffic. In order to reduce the complexity of having two real networks, we use the virtual channel policy of the ANOC router to split these two traffics. The request packets travels through the virtual channel VC0 while the response packets use the virtual channel VC1.

1.5) Limitations

The number of allowed hops in the network is limited to 9. Thus, the width and height of the network are conditioned to this limitation. The next equation have to be respected:

$$width_network + height_network - 1 \leq 9$$

2) Demonstrator platform

The basic multi_timer-mips32 platform has been implemented using the vci_anoc_network interconnect. This demonstrator platform can be found:

soclib/platform/topcells/caba-anoc-multi_timer-mips32 The vci_anoc_network module is located:

soclib/module/network_component/vci_anoc_network

This platform has been designed based on the DSPINPLUS implementation of the multi_timer-mips32 platform. The initial vci_dspinplus_network has been replaced by the vci_anoc_network.

