VciAvalonBus

1) Functional Description

This hardware component is a generic Avalon switchfabric allowing the interconnection of *Nb_Master* Avalon masters and *Nb_Slave* Avalon slaves. The master-to-slave relationship can be one-to-one, one-to-many, many-to-one, or many-to-many. Masters and slaves have the same data and address widths and operate in the same clock domain.

VCI-Avalon wrappers do not require to support full Avalon features, so not all Avalon slave and master ports are supported (AvalonSwitchMaster?, AvalonSwitchSlave?).

Implemented functionnalities :

- fundamental read, fundamental write with variable wait-state
- burst transfer
- flow control (dataavailable)
- round robin arbitration

Unimplemented functionnalities :

- wait state insertion
- pipelined read transfers
- tristate transfert
- setup and hold time
- dynamic bus sizing
- interrupt requests

2) Component definition & usage

3) CABA Implementation

CABA sources

- interface : source:trunk/soclib/soclib/module/network_component/avalon_switch_fabric/caba/source/include/avalon_switch_fab
- implementation : source:trunk/soclib/soclib/module/network_component/avalon_switch_fabric/caba/source/src/avalon_switch_fabric.c

CABA Constructor parameters

```
AvalonSwitchFabric (sc_module_name insname,                          // instance name
                    AvalonSwitchConfig<Nb_Master, Nb_slave> config)  // configuration
```

CABA Ports

- sc_in<bool> **p_resetn** : Global system reset
- sc_in<bool> **p_clk** : Global system clock
- AvalonSwitch_Master * p_avalon_master: Nb_Master ports from Avalon masters

- AvalonSwitch_Slave * p_avalon_slave: Nb_Slave ports to Avalon slaves

4) TLM-T implementation

There is no TLM-T implementation for this component.