VciDspin

The VciDspin interconnect is a low-cost, distributed network on chip, with a 2D mesh topology, providing the system designer a fully scalable bandwidth. It has been designed for shared memory clusterized, multi-processors architectures. It supports the GALS (Globally Asynchronous Locally Synchronous) approach. It implements a packet switching network, with a wormhole routing strategy, for low latency.

In order to avoid dead-locks for VCI command/response trafic it is strongly recommended to use two fully independent networks for the command packets and response packets: Each sub-system must contain the following hardware components:

- a VCI-DSPIN initiator wrapper
- a VCI-DSPIN target Wrapper
- a dedicated router for the command packets
- a dedicated router for the response paquets

A DSPIN network instanciates the three following components :

- VciDspinInitiatorWrapper
- VciDspinTargetWrapper
- DspinRouter