VciPibus

The VciPibus interconnect implements the PIBUS protocol.

- The VCI address and DATA fields must have 32 bits.
- The VCI fields PLEN, CONTIG, CONS, WRAP, CFIXED, CLEN are ignored.
- The supported PIBU response codes are PI_ACK_RDY, PI_ACK_WAT, and PI_ACK_ERR.
- The VCI initiator is supposed to be "fair" : when a command packet starts, the CMDVAL signal is true until the last word of the VCI packet (marqued by the EOP signal), and the RSPACK signal is supposed to be always true.
- The VCI command packet can have any length.
- Only the two VCI commands VCI_CMD_READ & VCI_CMD_WRITE are supported.
- Most output ports, including PI.A, PI.LOCK, VCI.RDATA, and VCI.RERROR are Mealy signals.

It is composed of three components :

- VciPiInitiatorWrapper : A VCI-PIBUS protocol converter for a VCI initiator.
- VciPiTargetWrapper : A VCI-PIBUS protocol converter for a VCI target.
- PibusBcu : A PIBUS controller for arbitration.