# VciPilnitiatorWrapper Functional Description

This hardware component is a VCI/PIBUS protocol converter. It behaves as an initiator on the PIBUS interface, and behaves as a target on the VCI interface. It can be used by a VCI initiator to interface a PIBUS based system on chip.

- The VCI address and DATA fields must have 32 bits.
- The VCI fields PLEN, CONTIG, CONS CLEN are ignored
- The supported PIBU response codes are PI\_ACK\_RDY, PI\_ACK\_WAT, and PI\_ACK\_ERR.
- The VCI initiator is supposed to be "fair" : when a command packet starts, the CMDVAL signal is true until the last word of the VCI packet (marqued by the EOP signal), and the RSPACK signal is supposed to be always true.
- The VCI command packet can have any length, but the VCI commands VCI\_READLOCK & VCI\_NOP are not supported.
- Most output ports, including PI.A, PI.LOCK, VCI.RDATA, and VCI.RERROR are Mealy signals.

# VciPiInitiatorWrapper CABA Implementation

The caba implementation is in

- source:trunk/soclib/systemc/include/caba/interconnect/vci\_pi\_initiator\_wrapper.h
- source:trunk/soclib/systemc/src/caba/interconnect/vci\_pi\_initiator\_wrapper.cc

## **Template parameters**

template<typename vci\_param>

### **Constructor parameters**

VciPiInitiatorWrapper( sc\_module\_name name); // Instance Name

### Ports

- sc\_in<bool> p\_resetn : Global system reset
- sc\_in<bool> **p\_clk** : Global system clock
- sc\_in<bool> **p\_gnt** : bus grant port (from the PIBUS contrioller)
- sc\_out<bool> **p\_req** : bus request port (to the PIBUS controller)
- soclib::caba::VciTarget<vci\_param> **p\_vci** : The VCI port
- soclib::caba::PibusInitiator **p\_pi** : The PIBUS port