VciXicu

1) Functional Description

This VCI target is a memory mapped peripheral implementing a vectorized interrupt controller, a timer controller, and an Inter-processor interrupt controller.

It can concentrate up to

- 32 independent interrupt lines
- 32 independent timers
- 32 IPI registers

multiplexing to up to 32 output lines

Complete specification is in xicu-1.0.pdf.

2) Component definition & usage

source:trunk/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/caba/metadata/vci_xicu.sd

```
Uses( 'vci_xicu' )
```

3) CABA Implementation

CABA sources

- interface : source:trunk/soclib/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/caba/source/include/vc
- implementation : source:trunk/soclib/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/caba/source/src/vci_xic

CABA Constructor parameters

```
VciXicu(
     sc_module_name name,  // Component Name
     const soclib::common::InTab &index, // Target index
     const soclib::common::MappingTable &mt,  // Mapping Table
     size_t pti_count,   // Number of programmeble timers
     size_t hwi_count,   // Number of hardware interrupt lines
     size_t wti_count,   // Number of write-triggerred interrupts (IPI)
     size_t irq_count);  // Number of output lines
```

CABA Ports

- sc_in<bool> **p_clk** : Global system clock
- sc_in<bool> **p_resetn** : Global system reset
- soclib::caba::VciTarget<vci_param> **p_vci** : VCI port
- sc_out<bool> ***p_irq** : Output interrupt ports (irq_count)
- sc_in<bool> ***p_hwi** : Input interrupts ports (hwi_count)