VciXicu

1) Functional Description

This VCI target is a memory mapped peripheral implementing a vectorized interrupt controller, a timer controller, and an Inter-processor interrupt controller.

This controller is an interrupt hub, concentrating 3 types of interrupts:

- up to 32 internal programmable timer interrupts (PTI),
- up to 32 external hardware interrupt lines (HWI),
- up to 32 internal write-triggered interrupts (WTI).

All these interrupt sources can be routed to up to 32 interrupt outputs. Each output can mask individual interrupt sources. Priority between interrupt source types is left to the handling operating system. Priority of interrupts inside an interrupt source type is from the lowestIdx(highest priority) to the highestIdx(lower priority).

Complete specification is in xicu-1.0.pdf.

1.1) Constructor Parameters

All hardware implementations of this component may not implement all the up-to-32 PTI (Timers), up-to-32 HWI lines, up-to-32 WTI registers and up-to-32 OUTPUTlines. The following parameters allow the system designer to get just the needed hardware.

- pti count (in range0..32): number of programmable timers
- hwi count (in range0..32): number of external hardware interrupt lines
- wti count (in range0..32): number of write-triggered interrupt sources
- irqcount (in range1..32): number of output interrupt lines

1.2) Programmers's View

This component can be mapped anywhere in the address space, on a 4-KiBboundary. This component is 32-bit data-word based: arbitrary byte access is not supported. 12 lower address lines are used the following way:

FUNC	INDEX	00
5 bits	5bits	

- **FUNC** indicates the functionnality
- **IDX** index in the range 0...31

MODE	Register	FUNC	INDEX
R/W	WTI_REG	00000	WTI_IDX
R/W	PTI_PER	00001	PTI_IDX
R/W	PTI_VAL	00010	PTI_IDX
W	PTI_ACK	00011	PTI_IDX
R/W	MSK_PTI	00100	0UT_IDX
W	MSK_PTI_ENABLE	00101	OUT_IDX

W	MSK_PTI_DISABLE	00110	OUT_IDX
R	PTI_ACTIVE	00110	OUT_IDX
R/W	MSK_HWI	01000	OUT_IDX
W	MSK_HWI_ENABLE	01001	OUT_IDX
W	MSK_HWI_DISABLE	01010	OUT_IDX
R	HTI_ACTIVE	01010	OUT_IDX
R/W	MSK_WTI	01100	OUT_IDX
W	MSK_WTI_ENABLE	01101	OUT_IDX
W	MSK_WTI_DISABLE	01110	OUT_IDX
R	WTI_ACTIVE	01110	OUT_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX
R/W	WTI_REG_WTI_IDX	00000	WTI_IDX

2) Component definition & usage

source:trunk/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/caba/metadata/vci_xicu.sd

```
Uses( 'vci_xicu' )
```

3) CABA Implementation

CABA sources

- interface : source:trunk/soclib/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/caba/source/include/vc
- implementation : source:trunk/soclib/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/caba/source/src/vci_xic

CABA Constructor parameters

```
VciXicu(
     sc_module_name name,  // Component Name
     const soclib::common::InTab &index, // Target index
     const soclib::common::MappingTable &mt,  // Mapping Table
     size_t pti_count,   // Number of programmeble timers
     size_t hwi_count,   // Number of hardware interrupt lines
     size_t wti_count,   // Number of write-triggerred interrupts (IPI)
     size_t irq_count);  // Number of output lines
```

CABA Ports

- sc_in<bool> **p_clk** : Global system clock
- sc_in<bool> **p_resetn** : Global system reset
- soclib::caba::VciTarget<vci_param> **p_vci** : VCI port
- sc_out<bool> ***p_irq** : Output interrupt ports (irq_count)
- sc_in<bool> ***p_hwi** : Input interrupts ports (hwi_count)

4) TLM-DT Implementation

TLM-DT sources

- interface :
  source:trunk/soclib/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/tlmdt/source/include/vc
- implementation :
  source:trunk/soclib/soclib/module/infrastructure_component/interrupt_infrastructure/vci_xicu/tlmdt/source/src/vci_xi

TLM-DT Constructor parameters

```
VciXicu(
     sc_module_name name,  // Component Name
     const soclib::common::InTab &index, // Target index
     const soclib::common::MappingTable &mt,  // Mapping Table
     size_t pti_count,   // Number of programmeble timers
     size_t hwi_count,   // Number of hardware interrupt lines
     size_t wti_count,   // Number of write-triggerred interrupts (IPI)
     size_t irq_count);  // Number of output lines
```

TLM-DT Ports

- **p_vci** : VCI target port
- **p_irq[irq_count]** : Output interrupt ports
- **p_hwi[hwi_count]** : Input interrupts ports