SoCLib components documentation

VCI Targets

- VciRam : A multi-segment embedded Ram controller
- VciMultiTty : A memory mapped multi-TTY controller
- VciMultiTimer : A memory mapped multi-Timer controller
- VciIcu : A memory mapped interrupt controller
- VciLocks : A memory mapped locks controller

VCI Initiators

- VciXcache : A generic data & instruction cache controller for RISC processors

Dedicated coprocessors (both targets and initiators)

- VciDma : A DMA engine
- VciFdAccess : A component wrapping access to simulator file descriptors
- VciMwmrController : A component allowing access to Mwmr channels

VCI Interconnects

- VciVgmn : A VCI advanced generic micro-network
- VciSimpleCrossbar : A VCI crossbar
- VciLocalCrossbar : A VCI crossbar with a dedicated port to connect to the global micro-network
- VciPiInitiatorWrapper : A VCI-PIBUS protocol converter for a VCI initiator
- VciPiTargetWrapper : A VCI-PIBUS protocol converter for a VCI target
- PibusBcu : A PIBUS controller
- VciRingInitiatorWrapper : A VCI-Ring controler for a VCI initiator
- VciRingTargetWrapper : A VCI-Ring controler for a VCI target
- RingRegister? : A pipe-line stage for a Ring interconnect

Processor wrappers

- IssWrapper : An ISS wrapper

Common utilities

- TtyWrapper : A simulator-side TTY abstraction tool, used by VciMultiTty
- MappingTable : A tool to declare and list all memory segments in a platform

Instruction Set Simulators

- Mips : Mips-R3000
- Ppc405 : PPC405
- MicroBlaze : Micro Blaze
- NiosII : NiosII