SoCLib components documentation

VCI Targets

- VciRam : A multi-segment embedded Ram controller
- VciMultiTty : A memory mapped multi-TTY controller
- VciMultiTimer : A memory mapped multi-Timer controller
- VciIcu : A memory mapped interrupt controller
- VciLocks : A memory mapped locks controller

VCI Initiators

- VciXcache : A generic data & instruction cache controller for 32 bits RISC processors
- VciDma : A DMA engine
- VciFdAccess : A component wrapping access to simulator file descriptors
- VciMwmrController : A component allowing access to Mwmr channels

VCI Interconnects

- VciVgmn : A VCI compliant generic micro-network
- VciLocalCrossbar : A VCI compliant crossbar
- VciPibus A VCI compliant PIBUS implementation
- VciRing? : A VCI compliant ring interconnect
- VciDspin : A VCI compliant DSPIN micro-network

Processor wrappers

- IssWrapper : A generic ISS wrapper, used to build CABA models for 32 bits RISC processors

Common utilities

- TtyWrapper : A simulator-side TTY abstraction tool, used by VciMultiTty
- MappingTable : A tool to declare and list all memory segments in a platform

Instruction Set Simulators

- Mips : Mips-R3000
- Ppc405 : PPC405
- MicroBlaze : MicroBlaze
- NiosII : NiosII