Processor ISS (Instruction Set Simulator)

These ISS must be wrapped in a CABA, TLM, or TLMDT wrapper to be used in a Soclib plat-form. Example of such a wrapper is the VciXcacheWrapper component.

- processors using the Iss2API
  - Mips32
  - Ppc405
  - Arm
  - Sparc v8
  - Lattice Micro 32

- processors using the IssAPI
  - MicroBlaze
  - NiosII
  - ARM7TDMI
  - ARM966
  - TMS320C62
  - MPC7447A

- Tools/Gdb Server : A GDB-server wrapper, for any ISS using the Iss2API.
- IssIss2 : Utility wrapper to use any IssApi compliant ISS in an Iss2Api wrapper

Components

VCI Targets

- VciRam : A multi-segment embedded Ram controller
- VciSimpleRam : A multi-segment embedded Ram controller with parameterized latency
- VciMultiTty : A memory mapped multi-TTY controller
- VciXicu : A memory mapped Hardware interrupt + Timer + IPI controller
- VciTimer : A memory mapped multi-Timer controller
- VciIcu : A memory mapped interrupt controller
- VciLocks : A memory mapped locks controller
- VciPCI : A bridge to the PCI bus
- VciLogConsole : A memory-mapped text log sink
- Mailbox : A mailbox component allows several processors to communicate via an interrupt mecanism

VCI Initiators

Iss Wrappers (caches)

- VciXcacheWrapper : A generic, VCI compliant, cache controller for Iss2Api processors
- VciCcXcacheWrapper : A generic, VCI compliant, cache controller for Iss2Api processors with directory-based cache coherence support
- VciVcacheWrapper : A generic, VCI compliant, cache controller for Iss2Api processors supporting virtual memory

Other initiators

- VciXcache : An old cache controller for 32 bits RISC processors (deprecated)
- VciDma : A DMA engine
- VciFdAccess : A file system access controller
- VciBlockDevice : A block device controller
- VciMwmrController : A Mwmr channels controller
- VciMwmrControllerLf : Another Mwmr channels controller

VCI Interconnects

- VciVgmn : A VCI compliant generic micro-network.
- VciVgsb : A VCI compliant generic system bus.
- VciLocalCrossbar : A VCI compliant crossbar.
- VciPibus : A VCI compliant PIBUS implementation.
- VciDspin : A VCI compliant DSPIN micro-network.
- VciSimpleRingNetwork : A VCI compliant ring interconnect.
- VciLocalRingNetwork : A VCI compliant ring interconnect.
- VciAvalonBus : A VCI compliant AVALON bus interconnect.
- VciAnoc : A VCI compliant ANOC micro-network.
- VirtualDspinNetwork : A VCI compliant Dspin micro-network with virtual channels.

Dedicated coprocessors

- Tc4200 : A WiMAX LDPC decoder
- Tc4200_enc : a WiMAX LDPC encoder
- trx_ofdm : A FFT and IFFT coprocessor
- FIR128 : A 128-taps Finite Impulse Response filter
- Upsampling : An interpolation component
- Downsampling : A decimation component
- Synchronization : A synchronization component
- Mapping : A mapping component
- Demapping : A demapping component
- FHT : A Fast Hartley Transform component

Common utilities

- MappingTable : A tool to declare and list all memory segments used in a platform and to define the memory mapping.
- Loader : A binary-file loader (ELF, COFF, plain)
- VciTargetFsm : A generic CABA submodule for handling the VCI fsm part of a target components, so that you can focus on the functionality
- TtyWrapper : A simulator-side TTY abstraction tool, used by the VciMultiTty component
- ProcessWrapper : A simulator-side fork/exec abstraction tool, with process' stdin/stdout communication
- FbController : A simulator-side framebuffer abstraction tool