About SoCLib design

ISS design

A Generic Instruction Set Simulator API for Timed and Untimed Simulation and Debug of MP2-SoCs At RSP'09, doi ?10.1109/RSP.2009.11

This paper presents a method for designing SystemC-compliantInstruction Set Simulators (ISS) that address three of the majorproblems system designers are faced with when modeling MP-SoCs architectures: the multiple levels of abstraction of the simulation models supporting the design space exploration, the simulation speed,and the debug of the multithreaded embedded application. First, this paper presents the ISS API and principles; then it describes howthe same ISS can support SystemC simulation at several abstraction levels: untimed transaction level, approximately timed transactionlevel, and cycle accurate; then, it describes how the proposed ISS API has been used by six different laboratories - in the framework of theSoCLib project - to share the same L1 cache simulation model, and towrap seven different processor cores in the same generic wrappers. Finally we demonstrate how the proposed API has been exploited to develop a generic debug and instrumentation infrastructure that can be used for all the processor cores, and allthe abstraction levels supported by the SoCLib virtual prototyping platform.