GAUT

General Presentation

GAUT is an academic High-Level Synthesis tool dedicated to Digital Signal Processing DSP applications.

Starting from a pure C function GAUT extracts the potential parallelism before selecting/allocating operators, scheduling and binding operations.

The mandatory design constraints are (1) the throughput (the initiation interval), (2) the clock period and (3) the target technology. The optional design constraints are I/O timing diagram and the memory mapping.

GAUT synthesizes a potentially pipelined architecture composed of a processing unit, a memory unit, a communication and multiplexing unit and a GALS/LIS interface.

GAUT generates an IEEE P1076 compliant RTL level VHDL file. This VHDL file is an input for commercial, off the shelf, logical synthesis tools like ISE/Foundation from Xilinx and Design Compiler from Synopsys.

More Information

You can obtain more detailed information, and download the tool ?here