SystemCass

General presentation

SystemCASS is a SystemC simulation engine, optimized to simulate hardware architectures modeled with the CABA (cycle accurate, bit accurate) components of SoCLib. This simulator is 15 times faster than OSCI's simulator (SystemC 2.1.v1).

Why is SystemCASS faster ?

SystemCASS takes advantage of the CABA modeling rules of the SoCLib project, to use static scheduling technics, and behave as a cycle-based simulator. During simulator elaboration, SystemCASS builds a signal dependency graph according to the architecture to simulate. The scheduler relies on this graph to statically compute the scheduling.

More Information

SystemCASS is an evolution of the CASS simulator developped by Frédéric Pétrot and Denis Hommais. It has neen developped at UPMC-LIP6 by Richard Buchmann & Alain Greiner, and is distributed as free software, under the GPL license.

You can obtain more detailed information, and download the code ?here