

Technical features

The main concern is true interoperability between the SoCLib IP cores :

- All simulation models are written in SystemC
- All SoCLib components respect the VCI / OCP communication protocol.
- Two types of models are available for each IPcore : CABA (Cycle Accurate / Bit Accurate), and TLM-T (Transaction Level Modeling with Time)

Availability

- All simulation models and most associated tools are distributed as free software.
 - The SoCLib documentation can be accessed [here](#)
 - To actually download one or several SoCLib tools or component, you must register below.
 - For each SoCLib component, a synthesizable RTL model is available, in order to guarantee a path to silicon, but this RTL model is NOT part of the SoCLib library, in order to preserve the IP providers business.
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Get your own copy

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Please note that this e-mail will be your login ID!

You may also want to sign-up for the developers mailing list dev@?, to do so please visit this [link](#).

If you need write access or for any other problem please contact.
