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What is SoCLib

- SoCLib is an open platform for virtual prototyping of multi-processors system on chip (MP-SoC).
- The project started as an ANR-funded project. It is now maintained at [?Lip6](#)
- The core of the platform is a library of SystemC simulation models for virtual components (IP cores)
- The main concern is true interoperability between the SoCLib IP cores
- All simulation models are written in SystemC, and can be simulated with the standard SystemC simulation environment.
- Two types of models are available for each IP-core:
 - ♦ CABA (Cycle Accurate / Bit Accurate),
 - ♦ TLM-DT (Transaction Level Modeling with Distributed Time)
- All [simulation models](#) and most associated tools are distributed as free software.

Using SoCLib

SoCLib Components

- [SoCLib Components General Index](#) : documentation about the available hardware components (IP cores)

Installation

- If you want to try SoCLib without going through the installation process, the [?SoCLib Virtual machine appliance](#) may help you !
- [Installation Notes](#) : how to install the SoCLib platform on your computer
- [Frequently asked questions](#) is useful when things goes wrong

Projects using SoCLib

- [?TSAR, Tera-Scale Architecture](#): a scalable, shared-memory, coherent MP2-SoC

Software support

Embedded Os support

SoCLib platforms are able to run several operating systems:

- [DNA/OS](#) : DNA/OS is a micro-kernel for MPSoCs. It supersedes MutekA, and still provides the POSIX thread API.
- [MutekH](#) : Exo-kernel based OS for classical and heterogeneous MPSoCs with POSIX threads support
- [NetBSD](#) : Highly portable Unix-like Open Source operating system
- [ecore](#) : An open source, royalty-free, real-time operating system intended for embedded applications.
- [RTEMS](#) : Real-Time Operating System for Multiprocessor Systems

SoCLib Tools

Various tools comes along with SoCLib to ease research and development:

- [DSX](#) : Design Space Exploration tool
- [SystemCASS](#) : Fast SystemC simulation kernel
- [SoCView](#) : Interactive simulation environment for debug and instrumentation
- [GdbServer](#) : A GDB server for multi-processor architectures
- [MemoryChecker](#) : A memory access error checker similar to valgrind.
- [GAUT](#) : A high-level synthesis tool allowing to generate automatically systemC CABA and TLM-T files.

Middleware

- [MWMMR](#) : Hardware / Software communication middleware

Tutorials

- [DSX tutorial](#): Motion-JPEG, MWMMR, MutekH, DSX, Design-space exploration
- [DNA Motion-JPEG and OS tutorial](#)

Development

Writing and design guides

- [General SoCLib Rules](#) : general rules regarding the SoCLib components.
- [Processor Modeling](#) : a general method to write generic processor models.
- [CABA Writing Rules](#) : rules to write SystemC CABA simulation models.
- [TLM-DT Writing Rules](#) : rules to write SystemC TLM-DT simulation models.
- [Critères Pour Plate-Forme TLM-T](#) : criteria defined for writing TLM-T simulation models.
- [CABA/TLM-DT Transactors](#) : general principles
- [Adding new components to the library](#) : the rules to follow to add a new IP core to the library.
- [Vci Protocol](#) : VCI protocol considerations in SoCLib

Building platforms

- Soclib Cc is the current build system for SoCLib platforms.
 - ♦ SoclibCc/DesignGuide is an attempt to justify the choices made in soclib-cc
 - ♦ Soclib Cc/And Modelsim describes how to use SoCLib CABA models in ModelSim, to make RTL+CABA co-simulation
 - ♦ Soclib Cc/Meta Data describes the metadata (.sd) file format
 - ♦ Soclib Cc/Soclib Conf describes the configuration file format

SoCLib Resources

Publications

See Papers And Publications.

Mailing list

The dev@? Mailing list is public and targets general discussion about SoCLib component development.

To join the list, either

- send an email to `dev-subscribe@soclib.fr`;
- see <http://www.soclib.fr/www/info/dev>.