Welcome to SoCLib project home page

- Enter technical part

What is ADAM

ADAM stands for ?Adaptive Dynamic Architecture for MP2SoCs?. It is a project that has submitted in may 2007 to the ANR (Agence Nationale de la Recherche), and accepted in October 2007. It has officially started in January 2008.

ADAM is a prospective research project that directly addresses the hot topic of MP2SoC self-adaptability to altered operating conditions, like loss of performance, appearance of faulty hardware resources, and temperature overhead. The architectures targeted by ADAM are MP2SoC, Massively Parallel MultiProcessor systems on chip (more than one hundred of processing elements) containing homogeneous functional blocks (all blocks can perform the work requested by the application), but structurally heterogeneous (with different and process dependant performances, electrical and timing characteristics and reliability). Taking simultaneously these problems into account is mandatory to ensure the reliability and competitiveness of embedded systems to come.

Three French laboratories with international reputation have joined their effort to propose a unified approach to the self-adaptability in MP2SoC issue. Considering a 2D mesh hardware architecture with a Network on Chip interconnecting clusters containing processing elements and local memories, the proposal can be summarized as a three steps process : non-intrusive online monitoring, online diagnosis/test, and online remapping. The main contribution of the ADAM project is to make these three steps finely interact through the use of onchip dynamic event databases: local databases of formatted/historized events and a global database of architecture instant maps, or architecture audited views classified by event types.

- ?Laboratoire d'Informatique de Paris 6
- ?CEA-LETI DCIS
- ?Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier

Technical features

The main concern is true interoperability between the SoCLib IP cores :

- All simulation models are written in SystemC
- All !SoCLib components respect the VCI /OCP communication protocol.
- Two types of models are available for each IPcore : CABA (Cycle Accurate / Bit Accurate), and TLM-T (Transaction Level Modeling with Time)

Availability

- All simulation models and most associated tools are distributed as free software.
- The SoClib documentation can be accessed ?here
- To actually download one or several SoClib tools or component, you must register below.
- For each SoCLib component, a synthesizable RTL model is available, in order to guarantee a path to silicon, but this RTL model is NOT part of the SoCLib library, in order to preserve the IP providers business.

Get your own copy

If you haven?t already done it, please register to create your account !

E-mail:

Please note that this e-mail will be your login ID!

You may also want to sign-up for the developers mailing list dev@?, to do so please visit this link.

If you need write access or for any other problem please contact.
