

Processor Functional Description

This hardware component is a Arm instruction set simulator.

This ISS uses the [ISS2 API](#) and can be wrapped in a CABA or TLM-T [Wrapper](#).

It implements most of the ARM-v6k instruction-set revision.

- Thumb is not supported yet.
- The floating point instructions are not supported
- Only little-endian variant is supported.
- This ISS implements the instruction set of ARM11, Cortex-M0, Cortex-M1

Component definition & implementation

- [source:trunk/soclib/soclib/iss/arm/metadata/arm.sd?](#)
- [source:trunk/soclib/soclib/iss/arm/include/arm.h?](#)
- [source:trunk/soclib/soclib/iss/arm/src/arm.cpp?](#)
- [source:trunk/soclib/soclib/iss/arm/src/arm_alu.cpp?](#)
- [source:trunk/soclib/soclib/iss/arm/src/arm_control.cpp?](#)
- [source:trunk/soclib/soclib/iss/arm/src/arm_coproc.cpp?](#)
- [source:trunk/soclib/soclib/iss/arm/src/arm_decoding_table.cpp?](#)
- [source:trunk/soclib/soclib/iss/arm/src/arm_instructions.cpp?](#)
- [source:trunk/soclib/soclib/iss/arm/src/arm_load_store.cpp?](#)

Template parameters

This component has no template parameters.

Interrupts

It has only one interrupt line.

Ports

None, it is to the wrapper to provide them.