DspinRouter

Functional Description

This hardware component is the generic router for the DSPIN micronetwork. It can be used in conjunction with the VciDspinTargetWrapper and the VciDspinInitiatorWrapper components to build a VCI compliant DSPIN micro-network. It implements a packet switching network, with a wormhole routing strategy, for low latency.

The DSPIN network on chip is a distributed network, with a 2D mesh topology. It has been designed for shared memory clusterized, multi-processors architectures. It supports the GALS (Globally Asynchronous Locally Synchronous) approach.

Component definition

Usage

CABA Implementation

- interface :
  source:trunk/soclib/soclib/module/network_component/vci_dspin_initiator_wrapper/caba/source/include/dspin_route
- implementation :
  source:trunk/soclib/soclib/module/network_component/vci_dspin_initiator_wrapper/caba/source/src/dspin_router.cpp

TLM-T implementation

There is no TLM-T implementation for the DSPIN network. (You can use the VciVgmn generic interconnect)

Template parameters

Constructor parameters

Ports