Processor Functional Description

This hardware component is a Sparc v8 processor core.

This ISS uses the ISS2 API and can be wrapped in a CABA or TLM-T Wrapper.

It implements all instructions defined in the Sparc v8 architecture specification, with the following limitations:

- LDSTUB, SWAP and alternate versions work only on a word granularity (see below)
- the ASI is currently not supported
- an optional FP is provided through a compilation flag (FPU, enabled by default)

Component definition & implementation

- source:trunk/soclib/soclib/lib/sparcv8/metadata/sparcv8.sd
- source:trunk/soclib/soclib/lib/sparcv8/include/sparcv8.h
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_run.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_logical.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_branch.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_load_store.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_traps.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_hazard.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_debug.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_fp.cpp
- source:trunk/soclib/soclib/lib/sparcv8/src/sparcv8_cp.cpp

Template parameters

This component has one template parameter :

- NWIN (int) : the number of windows. By default : 8

Interrupts

Sparc V8 defines 4 interrupts lines.

Ports

None, it is to the wrapper to provide them.

LDSTUB and SWAP support

SocLib infrastructure doesn't support directly SWAP and LDSTUB instructions. Thus they are emulated through SC and LL extended accesses. When executed, the infrastructure verify that they succeeded. If not, they may either trap or be automatically re-executed until successfull execution. The compilation flag SWAP_TRAPS decides which strategy to use. _Warning_ : when automatic re-execution is choosen, the system may deadlock.