Writing TLM2.0-compliant timed SystemC simulation models for SoCLib

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{{ #!html<h1>CABA/TLM-DT Transactors for the SoCLib virtual prototyping platform</h1> }}}

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This document is still under development.

1. A) Objetives

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The main goal of the CABA/TLM-DT transactors is to integrate a small number of CABA (Cycle Accurate Bit Accurate) simulation models in a TLM-DT simulation environment. More precisely, we make the assumption that the shared memory interconnect is a TLM-DT model. This mixed mode simulation, where CABA & TLM-DT simulation models are cooperating in the same simulation environment can be useful to validate a CABA model (versus a pre-existing TLM-DT model), or simply to build an heterogeneous top-cell if, or the TLM-DT models, either the CABA models are not available for some hardware components.